CMPEN 270 Fall 2016

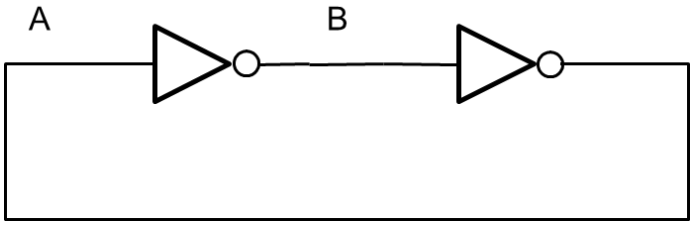
Assignment #4

Instructions

1. **The solutions to this assignment will need to be uploaded electronically as a TEXT, HTML or PDF document to the ANGEL course drop box. No paper copies will be permitted. Scanned handwritten submissions are OK if LEGIBLE.**
2. **All submitted work must be independent.**
3. **No late submissions will be accepted**
4. **For open-ended questions, you may refer to books or other publications but a reference and acknowledgment to the source is a MUST. Even in these cases, it is not acceptable to "verbatim" copy complete sentences from any source. You should always try to understand and use your own words.**

Due Tuesday, 11/1/16 @11:45pm

1) Given the simple memory element shown below:



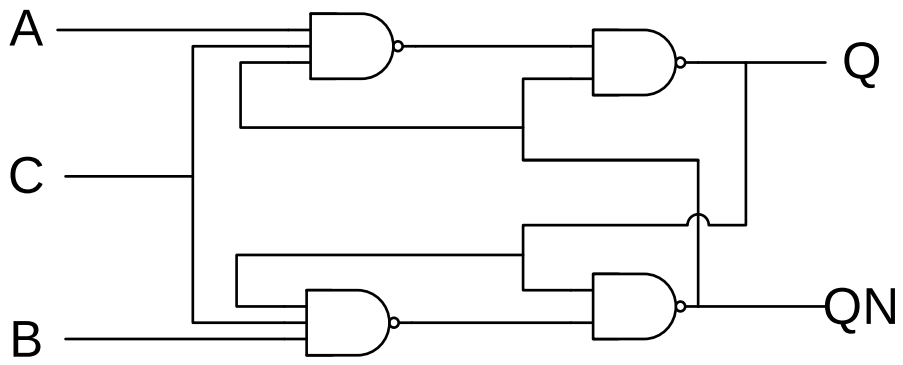
a) An engineer proposes to construct a memory element by using 3 series inverters instead of 2 (and the same output looped back to the input). Why does the boss believe that this is a bad idea?

b) The engineer, feeling very down after the boss's scolding thought very hard later that day and came up with another use for the 3-inverter circuit and regained all confidence. How can it be applied in a sequential circuit? It may help to sketch a few timing diagrams.

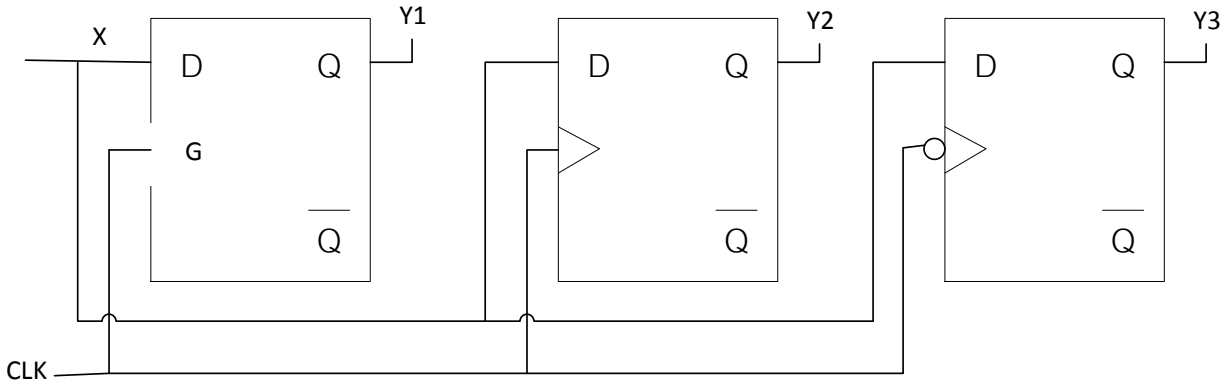
2) The circuit below is a slightly different SR latch than analyzed in your lecture.

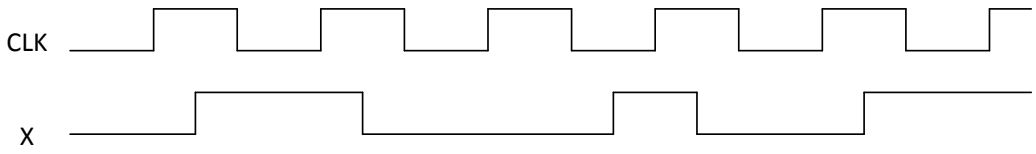
a) Obtain its truth table.

b) Draw the CMOS representation of the entire circuit using gates constructed from NMOS and PMOS transistors. PLEASE DRAW NEATLY.

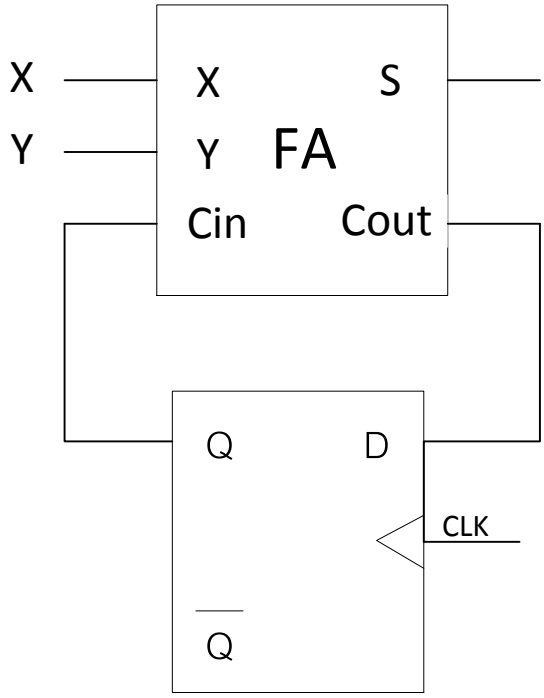


3) The circuit in figure contains a D – Latch, a positive edge triggered D flip-flop and a negative edge triggered D flip-flop. The signal X is applied to the input. Draw the waveforms of Y1, Y2, and Y3. Assume zero propagation delay between components.





4) Consider the full adder shown below with external inputs X and Y and Cin coming from the D flip-flop, which is fed by Cout. Obtain the state table showing the next states and output (S) and the state diagram of this circuit.



5) Counter design. Show all steps. Design a counter with the following binary sequence: 0, 1, 3, 7, 6, 4 and repeat. Use D-flip flops